REMARKS

At the time the Official Action was mailed, claims 1-36 and 38-50 were pending. Claims 1-36 and 38-50 stand rejected. Original claim number 37 was inadvertently omitted at the time of filing. Accordingly, original claims 38-50 have been renumbered as claims 37-49 and the dependencies in the claims have been renumbered as appropriate. Independent claims 1 and 40 (now claim 39) have been amended to cure minor deficiencies. . Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Objections to the claims

The Examiner objected to the claims based on the inadvertent omission of claim 37 at the time of filing and the misnumbering stemming therefrom. Accordingly, original claims 38-50 have been renumbered as claims 37-49 and those claims have been amended to recite proper dependency based on the renumbering, where appropriate. Applicant respectfully submits that these amendments are sufficient to overcome the Examiner's objection.

Amendments to Claims 1 and 40 (now claim 39)

While the Examiner did not object to or reject claims 1 or 43 (now claim 42) as lacking antecedent basis under 35 U.S.C. § 112, applicant has chosen to amend claim 1 and claim 40 (now claim 39), on which claim 43 (now claim 42) depends to set forth the recited subject matter more clearly and in order to circumvent any potential future rejections under 35 U.S.C. § 112. Specifically, "the first device interface" of claim 1 (line 12) has been amended to recite "the device interface." Further, because claim 43 (now claim 42) recites "the first device interface" and a "second device interface," claim 40 (now claim 39) has been amended such that line 10 recites "providing a first device interface."

Double Patenting Rejections

The Examiner rejected claims 1-50 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent Number 6,018,810. Accordingly, applicant hereby submits a properly executed terminal disclaimer in compliance with 37 C.F.R. § 1.321(b), attached hereto as appendix A. Applicant respectfully submits that the terminal disclaimer obviates the Examiner's obviousness-type double patenting rejection.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1-50 under 35 U.S.C. § 102(b) as being anticipated by Garbus et al. (U.S. Pat. No. 5,884,027), hereinafter "Garbus." Specifically, with respect to the independent claims, the Examiner stated:

> Garbus explicitly teaches:
> -a computer system [fig.2] comprising:
> -a host bus [abstract];
> -an input/output [I/O] fault-tolerant interconnect system [col.1, line12, fig.2]; and
> -a core logic chipset comprising a configurable bridge interface connectable between the host bus and the I/O fault-tolerant interconnect system [col.2, lines 15-20];
> -an I/O bus selectively comprising one of a first type bus and a second type bus, the I/O bus comprising a first bus portion and a second bus portion [fig.2, #17 the primary PCI bus is the first portion and #19, the secondary PCI bus is the second portion];
> -a device interface connectable to the I/O bus, wherein the first device interface is configured to detect errors in a transaction received by the device interface [col.6, lines 51-57; col.7, lines 17-21] wherein,
> -if a firs error is detected on the first bus portion, the transaction is performed over the second bus portion [col.16, table 4b];
> -if a second error is detected on the bus portion, then the transaction is performed over the first bus portion [col.17, table 4c].
>
> These claims are the same as per claims 1-8, 13-26. Therefore, these claims are also rejected under the same rationale applied against claims 1-8, 13-26.

Due to the similarity of claims 40-50 to claims 1-8, 13-26 except for a method of configuring a core logic chipset for connecting between a host bus and a fault-tolerant input/output bus instead a system one; therefore, these claims are also rejected under the same rationale applied against claims 1-8, 13-26.

Applicant respectfully traverses these rejections. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Because the Examiner rejected independent claims 27 and 40 (now claim 39) under the same rationale as applied to claim 1, the present response will specifically address those features explicitly recited in claim 1. However, based on the Examiner's rejection and the presently recited subject matter, it should be understood that the present response is directed to each of independent claims 1, 27 and 40 (now claim 39).

Applicant respectfully traverses the Examiner's rejection of claim 1 for at least two reasons. (1) First, Garbus does not disclose "an I/O bus selectively comprising one of a first type bus and a second type bus." (2) Second, the Garbus reference does not disclose performing a transaction over a portion of an I/O bus if an error is detected on an alternate portion of the I/O bus. More specifically, Garbus does not disclose a device interface connectable to an I/O

bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," and wherein "if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion."

With regard to the first point, claim 1 recites "an I/O bus selectively comprising one of a first bus type and a second bus type." As discussed in the background of the present specification, it would be desirable to provide a computer system having a core logic chipset *configurable* for either an accelerated graphics port (AGP) bus or a peripheral component interconnect (PCI) bus without requiring different logic and interface circuits for each *type* of bus. Specification, page 8, lines 15-17. The present invention advantageously provides a system configured for selecting an I/O bus type in the core logic chipset. Selection of the type of bus bridge (i.e., PCI or AGP) in the core logic chipset may be made by a hardware signal input, by software during computer system configuration or by a power on self test ("POST"). Specification, page 11, line 20 - page 12, line 1.

It is clear from the present specification that the *bus type* recited in claim 1 refers to one of an AGP bus or a PCI bus (which may comprise a PCI-X bus). This point is further clarified in claims 4 and 5. Specifically, claim 4 recites "wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus." Claim 5 recites "wherein the peripheral component interconnect bus comprises a PCI-X bus." As described in the present specification and recited in claim 1, the I/O bus is *selective* such that the I/O bus may be configured to comprise either of a first type of bus (e.g., AGP) or a second type of bus (e.g., PCI).

In contrast, Garbus discloses a primary PCI bus 17 and a second PCI bus 19. The Examiner correlated the presently recited first bus portion and second bus portion of the I/O

bus with the PCI buses 17 and 19 disclosed in Garbus. Specifically, the Examiner correlated the presently recited first portion of the I/O bus with the primary PCI bus 17 of Garbus and correlated the recited second portion of the I/O bus with the secondary PCI bus 19 of Garbus. However, the Examiner failed to cite any portion of Garbus that indicates that the I/O bus is selective between a first type bus and a second type bus, as also recited in claim 1. Indeed, if the Examiner is asserting that the primary PCI bus 17 of Garbus is comparable to the first portion of the I/O bus recited in claim 1 and that the secondary PCI bus 19 of Garbus is comparable to the second portion of the I/O bus recited in claim 1, the rejection is improper since it is clear that each of the buses 17 and 19 has the same bus type. Accordingly the I/O bus disclosed in Garbus can hardly be characterized as "*selectively* comprising one of a first type bus and a second type bus." Emphasis added. That is to say that each of the buses 17 and 19 disclosed in Garbus can be one and only one type of bus: a PCI bus. Accordingly, Applicant respectfully submits that Garbus does not disclose "an I/O bus selectively comprising one of a first type bus and a second type bus," as recited in claim 1.

Further, the Examiner rejected claim 4 in view of Garbus but failed to cite such a section of the Garbus reference that discloses a first type bus comprising an accelerated graphics port bus and the second type bus comprising a peripheral component interconnect bus. Indeed the Garbus references fails to make any mention of an AGP bus. For this additional reason, claims 4 and 5 cannot possibly be anticipated by the Garbus reference.

With regard to the second point, claim 1 recites a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," and wherein "if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion." As disclosed in the background of the present specification, it would be desirable to provide a system for improving fault tolerance

on an I/O bus when either of the upper (first) or lower (second) 32-bit data-width portions of a 64-bit data-width bus may have an operating fault. Specification, page 10, lines 19-22. In accordance with embodiments of the present invention, these problems are overcome by providing a fault tolerant 64-bit data-width PCI/PCI-X/AGP bus system which may recover from faults occurring on either the upper or lower 32-bit portions of a 64-bit data-width bus. Specification, page 11, lines 18-22. Thus, in accordance with one embodiment, the present invention provides a computer system having a fault tolerant 64-bit data-width PCI, PCI-X or AGP bus system that may recover from any fault occurring on either the upper or lower portions of the 64-bit data-width bus. Specification, page 19, lines 20-23. As recited in claim 1, if an error is detected on the first (e.g., upper) bus portion, then the transaction is performed over the second (e.g., lower) bus portion and vice versa.

With regard to these features of the device interface of claim 1, the Examiner cited tables 4b and 4c of Garbus. However, Applicant respectfully submits that *nothing* in the Garbus reference, much less tables 4b and 4c, indicate that if an error is detected on a first bus portion, the transaction is performed over the second bus portion. As previously described, the Examiner cited the primary PCI bus 17 as correlating with the recited first bus portion, and cited the secondary PCI bus 19 of the Garbus reference as correlating with the recited second bus portion. Assuming *arguendo* that this hypothetical correlation could be made, Garbus would necessarily have to disclose performing a transaction on the primary PCI bus 17 if an error is detected on the secondary PCI bus 19, in order to support a *prima facie* case of anticipation. The Examiner provided no citation of these characteristics as being disclosed in Garbus, and Applicant respectfully submits that Garbus does not disclose or teach a system having these characteristics. Accordingly, Applicant asserts that Garbus does not disclose a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed

over the second bus portion," or wherein "if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion."

For at least these reasons, Applicant respectfully submits that Garbus does not disclose each of the features recited in the present claims, and therefore, cannot possible anticipate the presently recited subject matter. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection under 35 U.S.C. § 102 and allowance of newly numbered claims 1-49.

Allowable Subject Matter

The Examiner indicated that claims 9-12, 31-34 and 43 (now claim 42) would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if a terminal disclaimer was filed to overcome the non statutory double patenting rejection. Applicant respectfully thanks the Examiner for the indication of allowable subject matter. However, for the reasons discussed above, Applicant respectfully submits that the present independent claims are also allowable and thus, have chosen not to amend claims 9-12, 31-34 and 43 (now claim 42) at this time.

Conclusion

In view of the remarks and amendments set forth above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of newly numbered claims 1-49. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 3/19/04

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